REMARKS

Applicants have carefully reviewed this Application in light of the Office Action mailed March 17, 2005. Claims 1, 6, 7, and 8 have been amended. Claims 4 and 5 have been cancelled. Claims 10-15 have been added. Thus, Claims 1, 2, 6-8 and 10-15 are pending in the application. Applicants respectfully request reconsideration and favorable action in this case.

Drawings

Replacement sheets and annotated replacement sheets are submitted to overcome the objection to the drawings.

With respect to Fig. 3, an additional amendment has been made by removing the dotted box labeled with numeral "6" to put this figure in conformity with Fig. 2.

Specification:

The Examiner objected to paragraph [0036] of the specification because of an informality. Applicants amended this paragraph according to the Examiner's objection.

Claim Rejections under 35 U.S.C. § 112

The Examiner objected to the claims because of informalities and because for failing to particularly point out and claim the subject matter. Applicants substantially amended all claims as will be explained below.

Claim Rejections under 35 U.S.C. § 103

Claims 1, 2, 5, 7, and 8 were rejected as being unpatentable over Kanai in view of Southard. Applicants substantially amended the claims to more clearly define the present invention. According to the present invention it is important to always provide for a synchronizing clock signal in certain applications, for example in automation system applications as explained in the background section of the application.

To this end, the present application proposes to provide for a special clock synchronization circuit. Generally, a predetermined number of clock pulses have to be generated between subsequent synchronization signals as a system clock signal. However,

phase shifts can occur or some synchronization signals might completely lack. Thus, the circuit according to the present invention provides two clock generation circuits. The first comprises a PLL circuit which receives the synchronization signals and generates a first clock signal comprising the predefined number of clock pulses between subsequent synchronization signals. The second clock generation circuit receives a phase regulating signal from the PLL. Thus, whenever the PLL operates in a locked mode, the output signal of the second clock generation circuit will be synchronous to the PLL circuit signal. In addition a phase comparison between the two output signal takes place and a stepwise adjustment is provided in case of a phase difference. However, if the PLL operates in an unlocked mode, then the second clock generation circuit will receive a predetermined control signal instead of the phase regulating signal to provide an independent clock signal.

Neither Kanai nor Southard provide for such a mechanism. In particular Southard generates clock signals from the same reference signal by means of two clock generators and compares the phases of the two separately generated signals. However, if the input clock reference signal fails, no output signal will be provided.

Claims 1, 2, and 4-8 were also rejected as being unpatentable over Alder in view of Finsterbusch. Applicants substantially amended the claims to more clearly define the present invention. As stated above, the present application proposes to provide for a special clock synchronization circuit.

Alder does not disclose such a clock circuit as defined in the independent claims. Alder proposes a clock generation unit with two PLL circuits that are interconnected. The first PLL generates a loop back frequency signal which is used as an input signal for the second PLL. Thus, this circuit does not comprise a control unit that receives a phase regulating signal. the phase regulating signal would be the signal within the first PLL that controls the oscillator VCXO. Also, Alder has no mechanism that distinguishes between a locked and an unlocked mode of the first PLL. Rather, Alder proposes to simply switch the loop back signal of the second PLL to the input of the first PLL in case the original input signal is not present.

Thus, Applicants believe that none of the cited prior art provides for the claimed mechanism. The dependent claims include all the limitations of the respective independent claims. Thus, these claims are allowable at least to the extent of the respective independent claims.

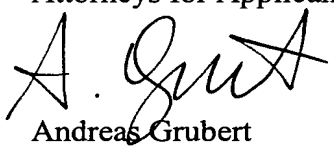
CONCLUSION

In light of the above remarks and amendments, reconsideration and withdrawal of the outstanding rejection is respectfully requested. It is further submitted that the application is now in condition for allowance and early notice of the same is earnestly solicited. Should the Examiner have any questions, comments or suggestions in furtherance of the prosecution of this application, the Examiner is invited to contact the attorney of record by telephone or facsimile.

Applicants believe no fees due at this time, however, the Commissioner is hereby authorized to charge any fees necessary or credit any overpayment to Deposit Account No. 50-2148 of Baker Botts L.L.P.

If there are any matters concerning this Application that may be cleared up in a telephone conversation, please contact Applicants' attorney at 512.322.2545.

Respectfully submitted,
BAKER BOTTS L.L.P.
Attorneys for Applicants



Andreas Grubert
Limited Recognition No. L0225
Expires June 30, 2006
(Limited Recognition under 37 C.F.R. §11.9(b))

Date: 10/27/05

SEND CORRESPONDENCE TO:
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Method for Controlled Synchronization to an Astable Clock System, and Reception Unit Corresponding Thereto
Inventors: Hendrik Rotsch, et al.
Attorney Docket.: 071308.0160
Annotated Drawings

FIG 1

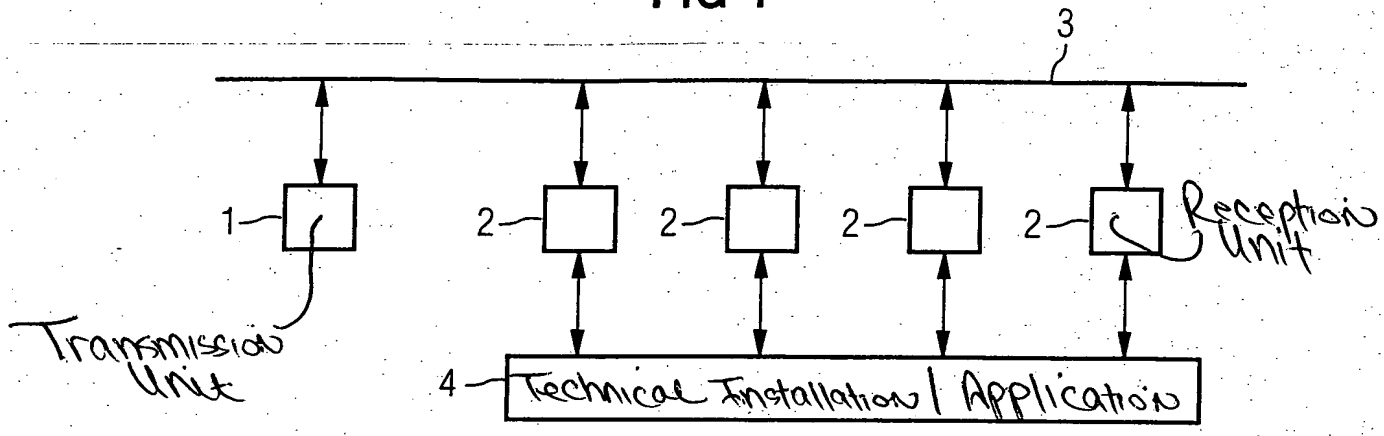

FIG 2

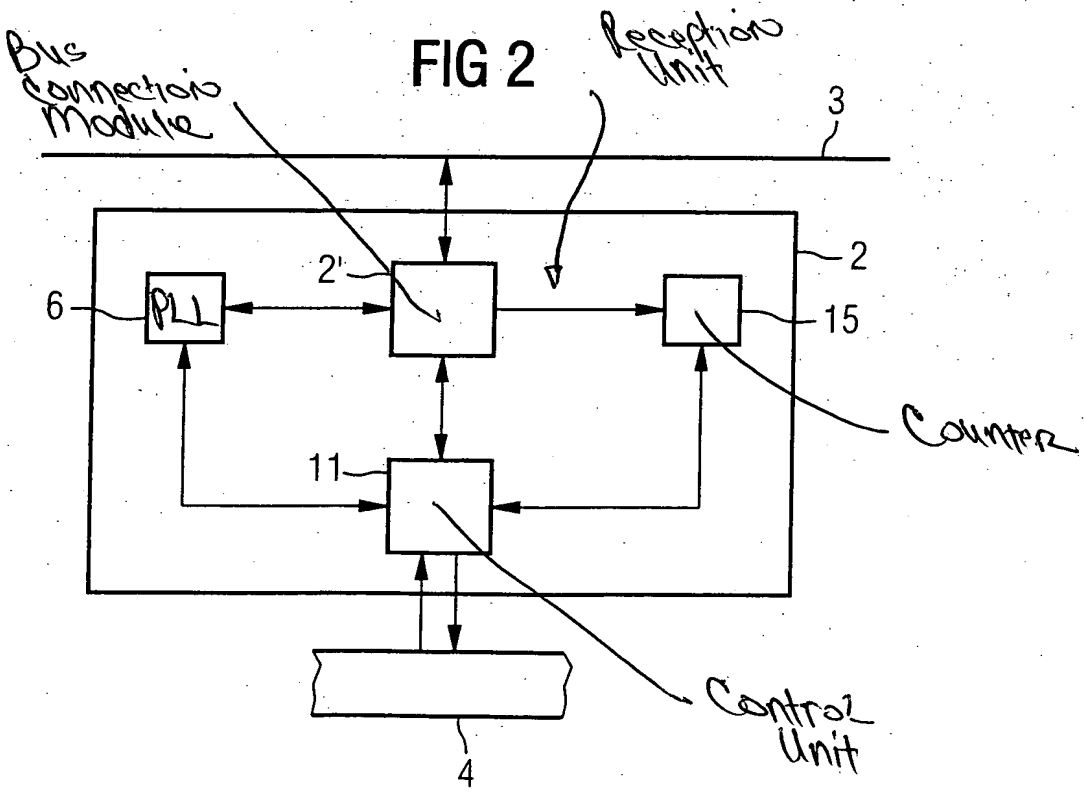

FIG 3

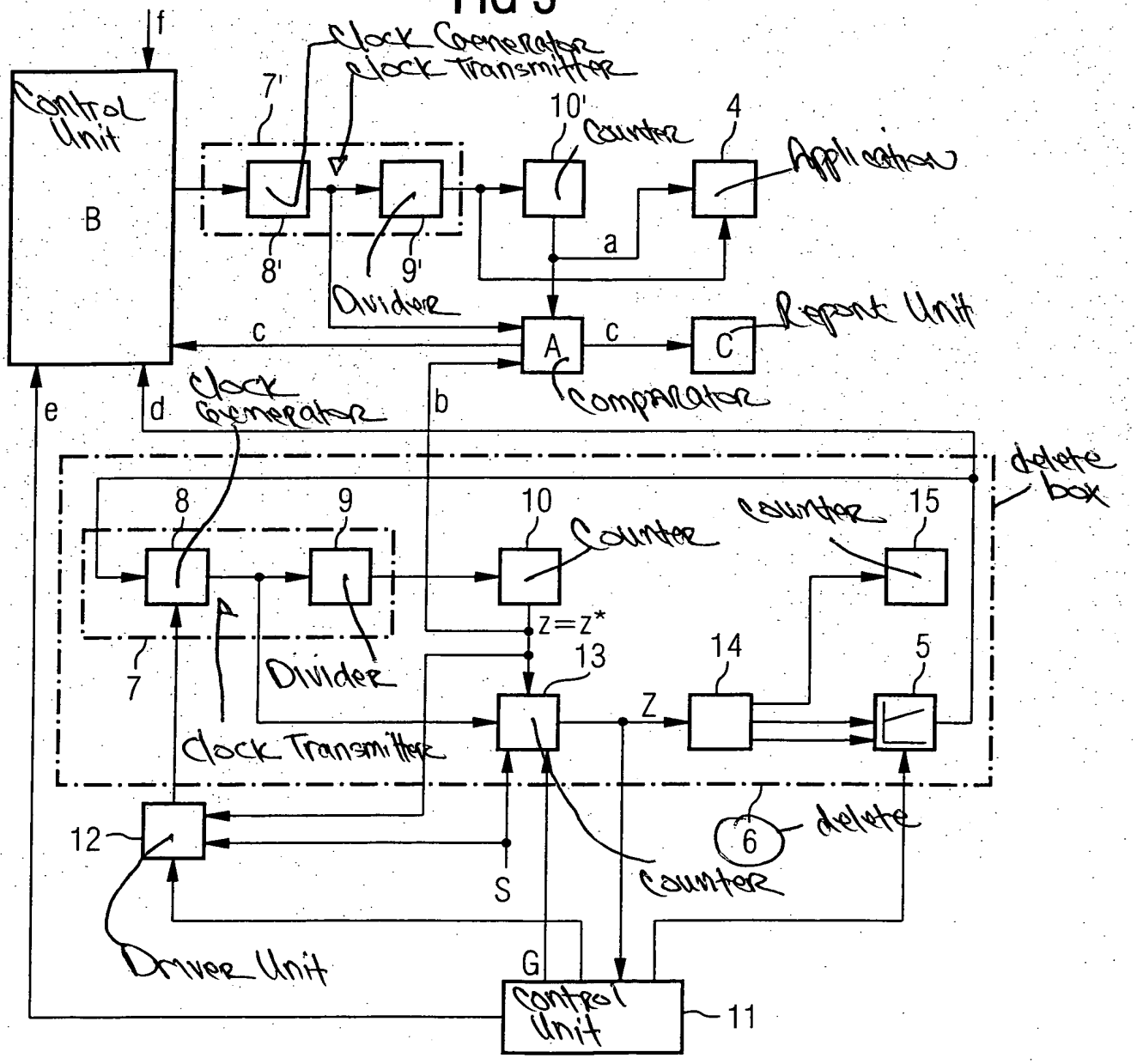
f
Control Unit
B
Clock Generator
Clock Transmitter
7'
8'
9'
Divider
10'
Counter
4
Application
a
c
A
Comparator
C
Report Unit
e
d
Clock Generator
b
delete box
8
9
10
Counter
15
Counter
7
Divider
z=z*
13
14
5
Z
Clock Transmitter
12
S
6
delete
Counter
Driver Unit
G
Control Unit
11

FIG 4